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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/802,468	03/16/2004	Ronald N. Perry	MERL-1559	4079

7590 03/23/2006

Patent Department
Mitsubishi Electric Research Laboratories, Inc.
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EXAMINER	
WASHBURN, DANIEL C	
ART UNIT	**PAPER NUMBER**
2628	

DATE MAILED: 03/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding..

Office Action Summary	Application No.	Applicant(s)	
	10/802,468	PERRY ET AL.	
	Examiner	Art Unit	
	Dan Washburn	2672	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/20/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments, see pages 2-6, filed 7/20/2005, with respect to the rejection(s) of claim(s) 1, 8, and 14 under Erlichson et al. (US 5,875,468) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Gaudette et al. (US 6,867,782).

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 12 recites the limitation "the set of caches" in line 2. There is insufficient antecedent basis for this limitation in the claim. Specifically, claim 8 describes a progressive cache, but does not explicitly describe a set of caches, and claim 12 does not describe a set of caches before referring to "the set of caches".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1-3, 5, 7-9, 11, 13, and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Gaudette et al. (US 6,867,782).

As to claim 1, Gaudette describes a system for processing data, comprising: a processing pipeline including a plurality of stages connected serially to each other so that an output element of a previous stage is sent as an input element to a next stage, and a first stage is configured to receive input for a processing request, and a last stage is configured to produce output corresponding to the input (column 1 lines 66-67, column 2 lines 1-17, and Figure 6 describe a processing pipeline. Figure 6 illustrates input clips 603 through 606 and processing stages 607 through 610, which are configured to receive input clips 603 through 606 upon receipt of an input frame

request, processing stages 609, 612, 613, and 602, which are connected serially to each other so that an output element of a previous stage is sent as an input to the next stage, and stage 601, which is configured to produce an output corresponding to the input); a progressive cache including a plurality of caches arranged in an order from least finished cache elements to most finished cache elements, each cache for receiving an output cache element of a corresponding stage and for sending an input cache element to a next stage after the corresponding stage (column 7 lines 33-45 and Figure 7 describe that all intermediate nodes can cache their processed image data, based on user specified caching requirements. Each intermediate node has a corresponding cache that receives an output element of a corresponding processing stage and can deliver this information to the next processing node in the processing pipeline upon request. This arrangement of caches is considered a progressive cache as caches corresponding to earlier processing stages, such as the cache associated with node 609 (Figure 6) contain the least processed, or least finished, cache elements, and caches corresponding to later processing stages, such as the cache associated with node 602, contain the most processed, or most finished, cache elements. Figure 5 and column 5 lines 22-35 describe the stages involved in processing an image); and a cache controller configured to route cache elements from the processing pipeline to the progressive cache in the order from a least finished cache element to a most finished cache element (column 10 lines 24-46 and Figure 12 describe an algorithm for accessing cache corresponding to a node. If a user has specified that a cache corresponding to a processing node is readable and writable then the algorithm, or

cache controller, will route the processed image data to the cache to be stored. This process is carried out for every node in the processing pipeline. Thus, the algorithm is considered a cache controller that routes cache elements from the processing pipeline to the cache in the order from least finished cache elements to most finished cache elements, as it stores least finished cache elements in the cache that is associated with the first set of processing nodes (607 through 610, of Figure 6), based on user specified caching requirements, and progressively works its way through the pipeline caching processed data until it caches the most finished cache elements with the last set of processing nodes (node 602), based on user specified caching requirements) and from the progressive cache to the processing pipeline in the order from the most finished cache element to the next stage after the corresponding stage (column 10 lines 46-58 describes that in rendering an image the process starts with the output node and works its way backwards through the processing nodes looking for cached data. If no cached data exists then the processing pipeline must begin processing the image from its initial state, but if cached data does exist then the search stops and the cached information is sent to the next stage in the processing pipeline for further processing. This is considered sending information from the progressive cache to the processing pipeline in the order from most finished cache element to the next stage after the corresponding stage, as the process starts with the output and works its way backwards through the processing stages looking for valid cached information to send to the next stage in the processing pipeline).

With regard to claim 2, Gaudette describes a system in which the progressive cache includes a cache for each stage of the processing pipeline (column 7 lines 33-45 describes that all intermediate nodes between input 701 (Figure 7) and output 704 can cache their output based on user specified caching requirements, which means that the user can potentially cache the result of every processing stage).

Concerning claims 3 and 9, Gaudette describes a method and system in which the output element is stored in the corresponding cache (column 7 lines 33-45 and column 8 lines 32-44 describe that the cache associated with each node has three states, read-only, read/write, and no reading or writing (effectively no cache). If a user sets the cache associated with each processing node to the read/write state then the system stores the output image data to the cache every time the output image data is altered at that node).

Regarding claims 5 and 11, Gaudette describes a method and system in which the cache elements are accessed by hashing (column 8 lines 45-67 describes that each node cache contains data for a user specified set of image frames. Each node has a tag corresponding to whether its cache has valid image data for a particular frame, and if a node indicates that its cache contains valid frame data then the system searches the cache to find the valid frame, which is considered accessing cached elements by hashing).

As to claim 7, Gaudette describes a system in which the input is a graphics object, and the output is an image (column 3 lines 35-45 describes taking source image

data, which is considered a graphics object, and processing it using any number of effects to create an output frame, or image).

With regard to claims 8 and 14, Gaudette describes a method and apparatus for processing data, comprising: receiving a processing request, the processing request describing input to be processed (column 6 lines 1-10 describes the system output sending a request for the next frame of information, the request works its way back through the processing nodes until valid image data is found in a cache or the request reaches the input to the processing pipeline); querying the progressive cache to determine a cached element most representing an output satisfying the processing request for input data (column 7 lines 51-67, column 8 lines 1-11, and Figure 8 describe caching image data at user specified nodes and then using the cached information that is furthest along in the processing pipeline the next time the same frame is displayed to shorten the amount of required processing time. This is considered querying a progressive cache to determine a cached element most representing an output satisfying the processing request); sending the cached element to a starting stage of a processing pipeline, the starting stage associated with the cached element (Figure 8 describes node 806, which is the starting stage of the processing pipeline that receives the cached image information from node 803); and sending an output of the starting stage as input to a next stage of the processing pipeline, a final stage of the processing pipeline determining the output satisfying the processing request for the input data (Figure 8 describes node 808, which receives the output of starting stage node 806 and

is a final stage of the processing pipeline determining the output satisfying the processing request).

Concerning claim 13, Gaudette describes a method wherein the starting stage associated with the cached element is a next stage of a corresponding stage of a cache of the progressive cache containing the cached element (Figure 8 describes that the cached information at node 803 is passed to processing node 806 upon request, node 806 has a corresponding cache, and node 806 and its associated cache are considered a starting stage and the next stage of the progressive cache for node 803 and its associated cache).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gaudette et al. (US 6,867,782) in view of Adl-Tabatabai et al. (US 2005/0071566).

Concerning claims 4 and 10, Gaudette describes a processing pipeline where each stage of the pipeline has a corresponding cache, as described in the rejection of claim 1. Gaudette doesn't describe a system or method wherein the cached elements are compressed.

However, Adl-Tabatabai describes a system and method for compressing cached elements (paragraphs 0023 and 0031-0033). It would have been obvious to

one of ordinary skill in the art at the time of the invention to include in Gaudette the system and method of compressing cached data, as taught by Adl-Tabatabai, in order to enable the storage of additional data within the same amount of area, which allows more frames of data to be stored in each cache in the system described in Gaudette. The advantage of storing more frames of data is that the system will have to process less unchanged information when outputting a sequence of frames, which means the system will be able handle a larger processing load of new information without lengthening the associated processing time.

Claims 6 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gaudette et al. (US 6,867,782) in view of Robertson et al. (US 5,956,744).

As to claims 6 and 12, Gaudette describes a processing pipeline where each stage of the pipeline has a corresponding cache, as described in the rejection of claim 1. Gaudette also describes that as cache space runs low the system uses a set of criteria to determine which portion of cache is not needed and should be overwritten (column 10 lines 59-67 and column 11 lines 1-40 describe prioritizing portions of cache based on number of times the cache is accessed, proximity to the output node, and other criteria). Gaudette doesn't describe a system and method wherein least recently used cache elements are discarded when the progressive cache is full.

However, Robertson describes a system and method in which the least recently used cached elements are discarded when the progressive cache is full (column 5 lines 60-67 and column 6 lines 1-24). It would have been obvious to one of ordinary skill in the art at the time of the invention to include in Gaudette the system and method of

discarding the least recently used cache elements, as taught by Robertson, in order to add the least recently used criterion to the set of criteria for replacing cache data disclosed in Gaudette. The advantage of adding the least recently used criterion to the set of criteria disclosed in Gaudette is that the system will be able to better predict the least valuable cache, which makes the use of cache space more efficient.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Cai et al. (US 6,470,422), Casamatta (US 6,243,794), and Deshpande et al. (US 6,442,597) describe multiprocessor multi-cache systems.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Washburn whose telephone number is (571) 272-5551. The examiner can normally be reached on Monday through Friday 8:30 a.m. to 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on (571) 272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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3/16/06

ULKA CHAUHAN
SUPERVISORY PATENT EXAMINER